ABSTRACT

A method and apparatus for a source synchronous address receiver for a system bus. In one embodiment, a flow-through between a system bus address input to a memory bus is controlled by two inputs: one is a source synchronous address strobe directing the receiver to latch the address and store data, while the other is a protocol signal, signaling the beginning of the address transfer. A flow-through circuit generates an enable signal in response to a digital address strobe signal and a digital address select signal to generate, prior to receipt of the address packet, an enable signal for a flow-through gate having the address packet and the enable signal as inputs. The flow-through gate provides the first component of the digital address packet (transaction address) to a chipset once the digital address packet appears on the address pin. Other embodiments are described and claimed.